FIRST PRELIMINARY AMENDMENT

November 16, 2001

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

In the Claims:

Please add the following new claims.

23. A method, comprising:

forming a first layer of spin-on glass on a substrate;

depositing a first dielectric on the first layer;

forming a second layer of spin-on glass on the first dielectric; and

planarizing the second layer of spin-on glass.

24. The method of claim 23 wherein forming the first layer of spin-on glass comprises depositing a siloxane-based spin-on glass on the substrate.

25. The method of claim 23 wherein forming the first layer of spin-on glass comprises depositing a polyimide spin-on glass on the substrate.

26. The method of claim 23 wherein forming the first layer of spin-on glass comprises depositing a polymethylmethacrylate spin-on glass on the substrate.

27. The method of claim 23 wherein forming the first layer of spin-on glass comprises curing the first layer at 425°C.

28. The method of claim 23, further comprising:

forming a second dielectric on the substrate before forming the first layer of spin-on glass; and

forming the first layer of spin-on glass on the second dielectric.

29. The method of claim 23, further comprising:

forming a layer of metal on the substrate before forming the first layer of spin-on glass; and

forming the first layer of spin-on glass on the layer of metal.

30. The method of claim 23, further comprising:

forming a layer of metal on the substrate before forming the first layer of spin-on glass;

depositing a second dielectric on the layer of metal before forming the first layer of spin-on glass; and

forming the first layer of spin-on glass on the second dielectric.

31. The method of claim 23 wherein depositing the first dielectric comprises performing a plasma-enhanced deposition of the first dielectric onto the first layer of spin-on glass.

32. The method of claim 23 wherein depositing the first dielectric comprises depositing an oxide onto the first layer of spin-on glass.

33. The method of claim 23 wherein depositing the first dielectric comprises depositing a low-temperature oxide onto the first layer of spin-on glass.

34. The method of claim 23, further comprising planarizing the first dielectric while planarizing the second layer of spin-on glass.

35. The method of claim 23, further comprising planarizing the first dielectric and the first layer of spin-on glass while planarizing the second layer of spin-on glass.

36. The method of claim 23 wherein planarizing the second layer of spin-on glass comprises etching back the second layer of spin-on glass.

37. The method of claim 23, further comprising:

wherein planarizing the second layer of spin-on glass comprises etching back the second layer of spin-on glass; and

etching back the first dielectric while etching back the second layer of spin-on glass.

38. The method of claim 23, further comprising:

wherein planarizing the second layer of spin-on glass comprises etching back the second layer of spin-on glass; and

etching back the first dielectric and the first layer of spin-on glass while etching back the second layer of spin-on glass.

39. A semiconductor structure, comprising:

a substrate;

a first layer of spin-on glass disposed on the substrate;

a first dielectric disposed on the first layer; and

a planarized second layer of spin-on glass disposed on the first dielectric.

40. The semiconductor structure of claim 39 wherein the first layer of spin-on glass comprises a siloxane-based spin-on glass.

41. The semiconductor structure of claim 39 wherein the first layer of spin-on glass comprises a polyimide spin-on glass.

42. The semiconductor structure of claim 39 wherein the first layer of spin-on glass comprises a polymethylmethacrylate spin-on glass.

43. The semiconductor structure of claim 39, further comprising:

a second dielectric disposed on the substrate; and

wherein the first layer of spin-on glass is disposed on the second dielectric.

44. The semiconductor structure of claim 39, further comprising:
a metal layer disposed on the substrate; and
wherein the first layer of spin-on glass is disposed on the metal layer.

45. The semiconductor structure of claim 39, further comprising:
a metal layer disposed on the substrate;
a second dielectric disposed on the metal layer; and
wherein the first layer of spin-on glass is disposed on the second dielectric.

46. The semiconductor structure of claim 39 wherein the first dielectric comprises a low-temperature oxide.

47. The semiconductor structure of claim 39, further comprising a planarized boundary that includes the planarized second layer of spin-on glass and a planarized portion of the first dielectric.

48. The semiconductor structure of claim 39, further comprising a planarized boundary that includes the planarized second layer of spin-on glass, a planarized portion of the first dielectric, and a planarized portion of the first layer of spin-on glass.

REMARKS

Claims 1 – 48 are pending in this broadening reissue application.

The Applicants have added new claims 23 - 48 to broaden the scope of protection to their invention.

The Applicants have added no new matter to the reissue application.

In light of the foregoing, original claims 1 – 22 and new claims 23 – 48 are in condition for full allowance, and that action is respectfully requested.

If the Examiner believes that a telephone interview would be helpful, he is respectfully requested to contact the Applicants' attorney, Bryan Santarelli, at (425) 455-5575.

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Respectfully submitted,

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